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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Transconductance circuit

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TRANSCONDUCTANCE CIRCUIT.

FIELD OF THE INVENTION

The present invention relates to a transconductance circuit intended to convert a differential input voltage, provided on two inputs, into a differential output current. More particularly, the invention relates to transconductance intended to be implemented in upconverter circuit and presenting a high linearity and a low noise.

BACKGROUND OF THE INVENTION

Such a highly linear differential transconductance is presented in the patent US5497123. This differential transconductance combines two sides each including a single input transconductance. Such a transconductance is a class AB transconductance. This class is advantageous as this is an intermediate between class A, where the consumption is independent from the processed signal, and class B, where there is a consumption only when a signal is processed. Advantages of class AB transconductance are also that they present a weak DC and are linear on a large range. Such a transconductance is presented for implementation in a reception chain. As such the transconductance exhibit a low input impedance to match with the image rejection filter output impedance. Consequently, the presented transconductance is well adapted to reception chain as the obtained gain is inversely proportional to the input impedance. A low input impedance is adapted to discrete applications where the input of the transconductance is an off-chip input.

For integrated applications the input impedance needs to be high in order to reduce the consumption. Moreover such a transconductance is not adapted to the use in transmission chains where a large and linear input impedance is generally asked for upconversion circuits.

SUMMARY OF THE INVENTION

The inventors have sought a design for a low noise highly linear class AB transconductance presenting a high input impedance.

This aim and others is reached with a transconductance circuit as presented in the introductory paragraph characterized in that, each of the two signals of said differential input voltage being provided to each input through a follower transistor connected to said input by its emitter and receiving said signal on a control electrode, each of the two inputs of the transconductance is connected to a respective current source that is dynamically controlled by the other input of the transconductance, said current source being such that the current provided to each input eliminates current variations caused by voltage variations of the input voltage signal.

The invention combines the use of a common collector stage realized through a follower transistor having its emitter connected to the input and the use of a positive feedback from one input to the other in order to cancel out current variations flowing in the follower transistors. Effectively, a simple follower transistor is not able to drive low input impedance with large input voltage. The combination with a current source providing a positive feedback enables to cancel large variations generated in the collector current of the follower transistor. Effectively these current variations modulate the base-emitter voltage of said follower transistor and hence introduce distortion unless it is drive with a very large current. A linear, low noise, high impedance class AB transconductance circuit is thus obtained.

An implementation of the invention is such that the transconductance circuit comprises two sides, each side comprising an input, an output, at least a first transistor having a control electrode coupled for receiving a bias voltage, a first electrode connected to said output and a second electrode connected to said input, a second transistor having a first electrode and a control electrode coupled in common to said input and a second electrode connected to a power supply terminal.

Advantageously, said first and second transistors are of the same size.

In an implementation of the invention, each side further including a third transistor of the same size than said second transistor, said third transistor having a control electrode, coupled to said first and control electrodes of said second transistor,

a first electrode connected to the output of the other side and a second electrode connected to said power supply terminal.

Such an implementation is known for providing a high linearity of the transfer function of the transconductance for large input voltage. As said third transistor is of the sama size than said second transistor, the transfer function is symetrical to both negative and positive input voltages.

First transistor handles very large amount of current during negative excursion of the input voltage. At the opposite, second and third transistors handle a very large amount of current during positive excursion of the input voltage. Acting together, these transistors provide a transfer function which is linear to both positive and negative input voltages whatever is the relative size of said first and second transistors. In a simple implementation, the first and second transistors are of the same size.

An implementation of the current source is thus such that said current source includes a current mirror mirroring the current passing through said second transistor with a gain of two. For instance, said current mirror includes a mirror transistor of twice the size of said second transistor, said mirror transistor having a control electrode connected to the first and control electrodes of said second transistor, a first electrode connected to the input of the other side and a second electrode connected to said power supply terminal.

The invention also relates to a chip intended to be implemented in a transmission chain and to a transmission device including such a chip.

These and other aspects of the invention will be apparent from and will be elucidated with reference to the embodiments described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be described in more detail, by way of example, with reference to the accompanying drawings, wherein:

- Fig. 1 is a schematic diagram of a transconductance as described in the prior art;
- Fig. 2 is a schematic diagram of an implementation of a transconductance according to the invention;

- Fig. 3a represents transfer functions of a transconductance according to the prior art and according to the invention;
- Fig. 3b represents the ouput currents for a transconductance of the invention;
- Fig. 4 represents a graph illustrating the performances of a transconductance according to the invention;
- Fig. 5 schematically represents a chip according to the invention;
- Fig. 6 represents a block diagram of a transceiver of radio frequency signals according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig.1 represents a transconductance circuit of the prior art. This transconductance circuit has two inputs IN+, IN- for receiving an input differential signal, and outputs OUT+, OUT- for providing a differential output signal. It includes two symetrical sides each comprising three transistors T1+,T2+,T3+ for the first side and T1-,T2-,T3- for the second side. Said transistors are bipolar or MOS transistors having a collector, a base and an emitter respectively corresponding to a first electrode, a control electrode and a second electrode.

Transistors T1+ and T1- have a control electrode coupled for receiving a bias voltage, a first electrode connected to said output, respectively OUT+ and OUT-, and a second electrode connected to said input, respectively IN+ and IN-, biased by a constant current Ibias.

Transistors T2+ and T2- are in a diode configuration having a collector and base coupled in common and an emitter coupled for receiving a power supply voltage (e.g. ground) from a power supply terminal PST.

Transistors T3+ and T3- have a control electrode coupled to said first and control electrodes of said second transistor, respectively T2+ and T2-, a first electrode connected to the output of the other side, respectively OUT- and OUT+, and a second electrode connected to said power supply terminal PST.

Connections of these transistors to the power supply terminal and to the input or output of the circuit may be realized through resistors. For example, on Fig. 1, connection of second electrode of said first transistors T1+ and T1- to the input is

realized through resistors R1+ and R1-. Connections of said second and third transistors to the power supply terminal PST are realized through resistors R2+,R2- and R3+,R3-. Said resistors have equal value by pairs and it is advantageous that they all have the same value. Such a remark is also applicable for the transconductance circuit of the invention represented on Fig.2.

An input signal having a positive incursion in voltage relative to a bias point Vbias applied, for example, to input IN+ reduces the voltage across the base emitter junction of transistor T1+. Conversely a voltage across the base-emitter junction of transistor T2+ is increased. Transistor T3+ is a mirror transistor of a current mirror circuit formed by transistors T2+ and T3+. The increase in base-emitter voltage of transistor T2+ is mirrored to transistor T3+ which increases a current provided at output OUT-.

Meanwhile, on the other side, an input signal having a negative incursion in voltage relative to a bias point Vbias is provided to input IN-. It has the opposite effect. A voltage across the base-emitter voltage of transistor T1- is increased by the negative voltage. Conversely, a voltage across the base-emitter junction of transistor T2- is decreased. The input signal having a negative voltage results in an increase in current at output OUT- and a decrease in current at ouput OUT+. The effects of the two sides of the transconductance go in the same way.

This transconductance continues to perform linearly under extreme conditions where the signal current is equal or bigger than the bias current and is not limited by a current source that bias the circuit. On each side, either transistor T1 or transistor T2 is turned off due to large input voltage. For example, an input signal having a large positive voltage applied to input IN+ turns off transistor T1+ but increases the current through transistor T2+ which is mirrored to the output OUT-. This output OUT- also receives the current from T1- while T2- is turned off. Effectively a large negative voltage applied to input IN- turns off transistors T2- and T3- but linearly increases the current through transistor T1- which is provided at ouput OUT-. Thus, the transconductance remains linear even under large negative or positive input voltage swings.

Nevertheless, as stated above, this transconductance has a low input impedance. An adaptation of the impedance could be done at each input IN+ and IN- of said transconductance. The elements of such an adaptation of impedance, if active, present the drawbacks to add distortion to the input signal. Indeed, the current variations flowing in the active, and thus non linear adaptative circuit, generate distortion.

The effect of a signal δv of the input voltage is shown on Fig.1. Such a voltage variation $+\delta v$ provided on IN+ results in a current variation δi in each of the two transistors T1+ and T1-. This current variation is then mirrored and an amplified variation of $2\delta i$ is obtained on output OUT+. A current $I_o+2\delta I$ or $I_o-2\delta i$ needs to be provided or absorbed by the impedance adaptation elements as the input is biased by a constant current Ibias. The impedance adaptation elements will consequently increase this variation and add distortion. For example, when the adaptation is realized through an emitter follower transistor, the base-emitter voltage of said follower transistor should consequently change, leading to distortion. Moreover, it makes the noise contribution from the adaptative circuit high when this circuit is momentarily biased at a low current.

Fig.2 represents an exemplary implementation of a transconductance of the invention that does not suffer from the above-presented drawbacks.

According to the invention, each of the two signals of said differential input voltage are provided to each input, respectively IN+ and IN-, through a follower transistor, respectively TF+ and TF-, connected to said input, respectively IN+ and IN-, by its emitter and receiving said signal on a control electrode. Moreover, each of the two inputs, respectively IN+ and IN-, of the transconductance is connected to a respective current source, respectively CS- and CS+, that is dynamically controlled by the other input of the transconductance, respectively IN- and IN+. Said current source, respectively CS- and CS+, is such that the current provided to each opposite input, respectively IN+ and IN-, by said respective current source, respectively CS- and CS+, eliminates current variations $2\delta i$ caused by voltage variations $+\delta v$ and $-\delta v$ of the input voltage signal.

A positive feedback is thus implemented so as to provide the input with a current equal in magnitude to the one absorbed. The resulting input impedance Zin is then very high. Effectively, a signal δv generating a weak current signal $\delta I=2\delta i-2\delta i$, the input impedance seen by the follower transistor $Zin=\delta v/\delta I$ is very high. The follower transistor TF has no longer current variations to provide to the input of the transconductance and does not generate any distortion even at high input voltages.

In the following the functioning of the left side of Fig.2 will be disclosed. The description of the functioning of the right side is similar. On Fig.2, the case where resistors R1+, R2+ have identical values and where transistors T1+, T2+ have the same size is illustrated. As seen previously, a voltage variation $+\delta v$ generates a current that is splitted half in the branch including T1+ and half in the branch including T2+. Consequently two current variations δi are generated in each branch. The current variations δi generated in T2+ is mirrored by T3+ to output OUT-. The effect of this current variation δi on output OUT- is additive with the effect of the current variation generated in the branch including T1-. The same phenomenon is observed on OUT+ as the current variation δi generated through T2- is mirrored by T3- towards the output OUT+.

Fig.2 proposes an exemplary implementation of the current source, respectively CS+ and CS-. Said current sources CS+ and CS- each includes a current mirror including a mirror transistor, respectively TM+ and TM-, having a control electrode connected to the first and control electrodes of said second transistor, respectively T2+ and T2-, a first electrode connected to the input of the other side, respectively IN- and IN+ and a second electrode connected to said power supply terminal PST.

The current is mirrored with a gain of two in order to cancel the current variations entering at the opposite input. Transistors TM+ and TM- of a size that is the double of the size of T2 may thus be used. In practice, where transistors do not present an ideal behaviour, the size of said mirror transistor TM is adapted depending the required range of output current. The connections of said mirror transistor TM+ and TM- to said power supply terminal may be realized through resistors RM+ and RM-. Such resistors are advantageously of the same value than the ones used with said

second and third transistors. A transconductance according to such an implementation presents a high input impedance symetrical to both positive and negative large voltage swings and a good linearity as illustrated on Fig.3a for a bias current of 5mA. The prior art transfert function illustrated by curve PAC is observed to be less linear than the invention transfer function illustrated by curve IC. The transconductance of the invention is shown to be linear even for high output current. Fig.3b represent the two ouput currents I(OUT+) et I(OUT-) for the transconductance of the invention. Each output current is not linear but the output differential current I(OUT+)-I(OUT-)=Idiff is perfectly linear.

Indeed, each input of the transconductance, respectively IN+ and IN-, is directly biased by the feedback realized through the opposite current sources, respectively CS- and CS+, instead of being biased by a constant current source.

The performances of the invention are illustrated on Fig.4. This figure shows the results of a two tones analysis performed on the implementation of the prior art, illustrated on Fig.1 and on the implementation of the invention presented on Fig.2. The first tone is a differential voltage having an amplitude V and a frequency of F1=375MHz and the second tone is a differential voltage of the same amplitude V and of a frequency of F2=385MHz. These two tones are injected at the inputs of the transconductance. At the ouputs of the transconductance, two main tones in current, IM1F1 and IM1F2, are obtained at the respective frequencies F1 and F2. Two secondary tones in current, IM3F1 and IM3F2, are also obtained at frequencies F1'=365MHz and F2'=395MHz. These secondary tones result from the non linearities of the transconductance. On Fig.4 are represented the tone IM1F1 for the frequency F1 and the difference between the tones IM1F1 and IM3F1 for frequency F1. The higher this difference is, the most the transconductance linear is. Curves for F2 would be similar. It is thus observed that, at identical bias current, for large input and output signals, the transconductance of the invention is more linear than the one of the prior art. This is illustrated by the fact that the difference IM1F1-IM3F1 is larger and that the slope of IM1F1 representing the gain of the transconductance does not fall for high input voltages. Moreover the transconductance of the invention is observed to be higher than the one of the prior art. This is illustrated by the gain expressed by the

IM1F1 curve. For example, it is observed that a transconductance of the invention can generate two differential tones having an amplitude of 15 mA with a difference IM1F1-IM3F1 of 40dB and a global bias current of only 10mA. The two differential tones are obtained with a gain variation below 1dB. The difference IM1F1-IM3F1 is 12dB higher than the one obtained with the prior art at small signal levels and is even larger (up to 26dB) at large input voltage.

Fig.5 illustrates a chip FTCT intended to be implemented in a transceiver according to the invention. Said chip includes at least a transconductance TRCD as previously described and a mixer circuit MIX dedicated to provide a frequency shifted signal from the current output from said transconductance TRCD.

Fig.6 illustrates a block diagram of a transceiver FCS of radio frequency signals according to the invention. Generally such a transceiver FCS is intended to receive and to transmit signals through an antenna ANT. A commutation device COM controls the access to the antenna ANT. Said commutation device COM is connected at least to a reception chain RX and to a transmission chain TX. Said reception chain RX includes at least a signal processing circuit SPC and a frequency translation unit FTCR, generally constituted of mixer circuits. A processing unit MC follows these circuits. This processing unit MC also processes the signals to be transmitted and is thus connected to a transmission chain TX that includes at least a frequency translation unit FTCT implemented in a chip as previously described in Fig.5 and an amplification unit AMPT. Such a transceiver is advantageously a telecommunication apparatus: mobile phone... Int his exemplary application of the invention, the invention takes place in an upconverter circuit for which the characteristocs of the invention are particularly well adapted.

It is to be understood that the present invention is not limited to the aforementioned embodiments and variations and modifications may be made without departing from the spirit and scope of the invention as defined in the appended claims. In the respect, the following closing remarks are made.

It is to be understood that linearity of the transconductance can also be modulated classically through the values of the resistors of the transconductance. Notably, modifications of the value of R_o enables such an improvement.

It is to be understood that isolation means can also be added to a circuit of the invention. For example, a transistor can be implemented in cascode with said third transistor, between the collector of said third transistor and the opposite output. This enables to avoid disturbances caused by a charge of said transconductance, for example, a mixer circuit.

It is to be understood that the invention is not limited to the aforementioned telecommunication application. The invention can be used within any application using a reception chain needing a frequency translation before further processing. Radio frequency application are thus very concerned by the invention.

It is to be understood that the present invention is not limited to the aforementioned mobile phone application. It can be used within any application using a system where a drift frequency occurs, in automobile application for example.

It is to be understood that the method according to the present invention is not limited to the aforementioned implementation.

Any reference sign in the following claims should not be construed as limiting the claim. It will be obvious that the use of the verb "to comprise" and its conjugations do not exclude the presence of any other steps or elements besides those defined in any claim. The article “a” or “an” preceding an element or step does not exclude the presence of a plurality of such elements or steps.

CLAIMS

1 A transconductance circuit intended to convert a differential input voltage, provided as two signals on two inputs, into a differential output current, characterized in that, each of the two signals of said differential input voltage being provided to each input through a follower transistor connected to said input by its emitter and receiving said signal on a control electrode, each of the two inputs of the transconductance is connected to a respective current source that is dynamically controlled by the other input of the transconductance, said current source being such that the current provided to each input by said current source eliminates current variations caused by voltage variations of the input voltage signal.

2 A transconductance circuit as claimed in claim 1, wherein the transconductance circuit comprises two sides, each side comprising an input, an output, at least a first transistor having a control electrode coupled for receiving a bias voltage, a first electrode connected to said output and a second electrode connected to said input, a second transistor having a first electrode and a control electrode coupled in common to said input and a second electrode connected to a power supply terminal.

3 A transconductance circuit as claimed in claim 2, wherein said first and second transistors are of the same size.

4 A transconductance circuit as claimed in one of claims 2 and 3, wherein each side further includes a third transistor of the same size than said second transistor, said third transistor having a control electrode coupled to said first and control electrodes of said second transistor, a first electrode connected to the output of the other side and a second electrode connected to said power supply terminal.

5 A transconductance circuit as claimed in one of the claims 2 to 4, wherein said current source includes a current mirro mirroring the current passing through said second transistor with a gain of two.

6 A transconductance circuit as claimed in claim 5, wherein said current mirror includes a mirror transistor of twice the size of said second transistor, said mirror transistor having a control electrode connected to the first and control electrodes of said second transistor, a first electrode connected to the input of the other side and a second electrode connected to said power supply terminal.

7 A chip intended to be implemented in a transceiver including at least a transconductance as claimed in one of the claims 1 to 6.

8 A transceiver of radio-frequency signals including at least one chip as claimed in claim 7.

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TRANSCONDUCTANCE CIRCUIT.

ABSTRACT

The present invention relates to a transconductance circuit intended to convert a differential input voltage, provided as two signals on two inputs, respectively IN+ and IN-, into a differential output current. According to the invention, each of the two signals of said differential input voltage are provided to each input, respectively IN+ and IN-, through a follower transistor, respectively TF+ and TF-, connected to said input, respectively IN+ and IN-, by its emitter and receiving said signal on a control electrode. Moreover, each of the two inputs, respectively IN+ and IN-, of the transconductance is connected to a respective current source, respectively CS- and CS+, that is dynamically controlled by the other input of the transconductance, respectively IN- and IN+, said current source, respectively CS- and CS+, being such that the current provided to each input, respectively IN+ and IN-, by said respective current source, respectively CS- and CS+, eliminates current variations caused by voltage variations of the input voltage signal.

Reference: Fig.2

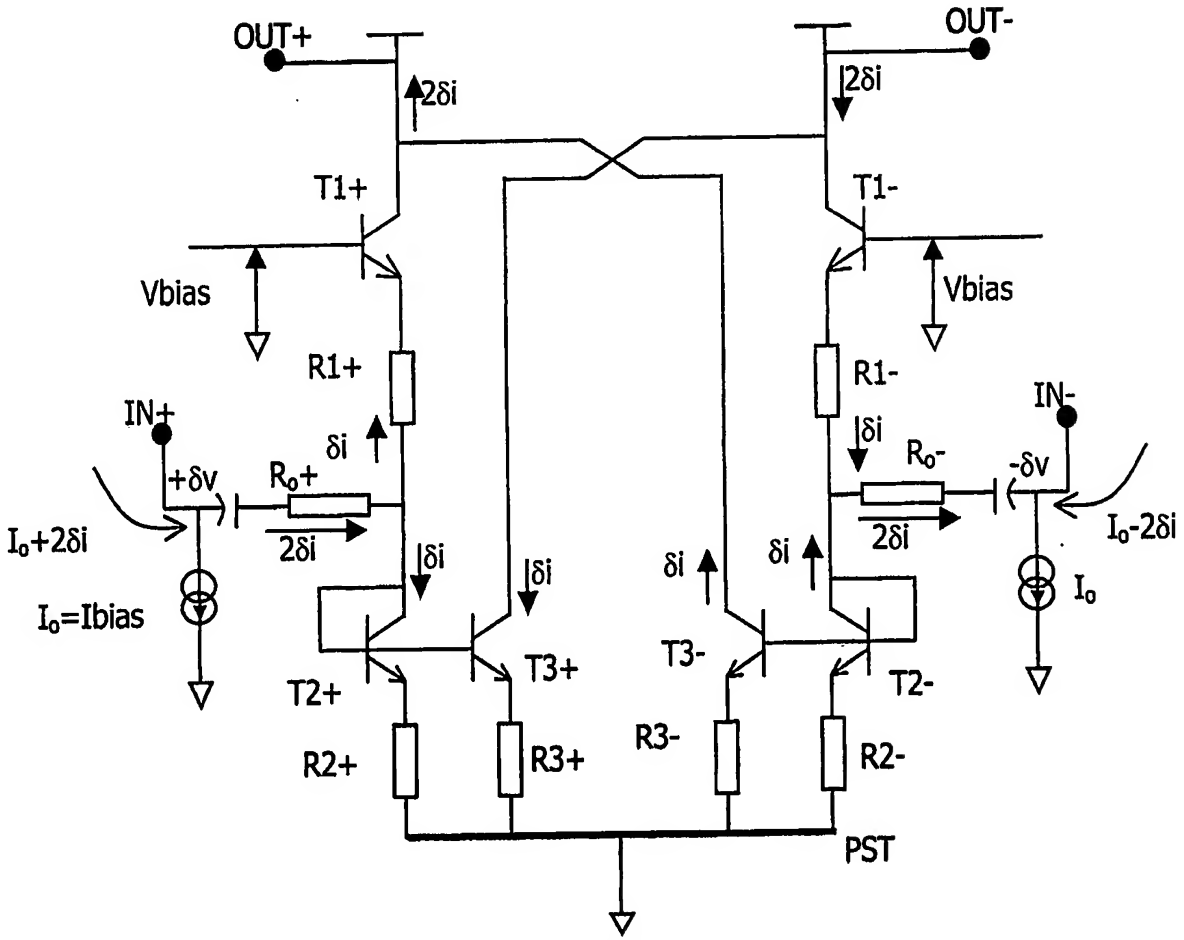
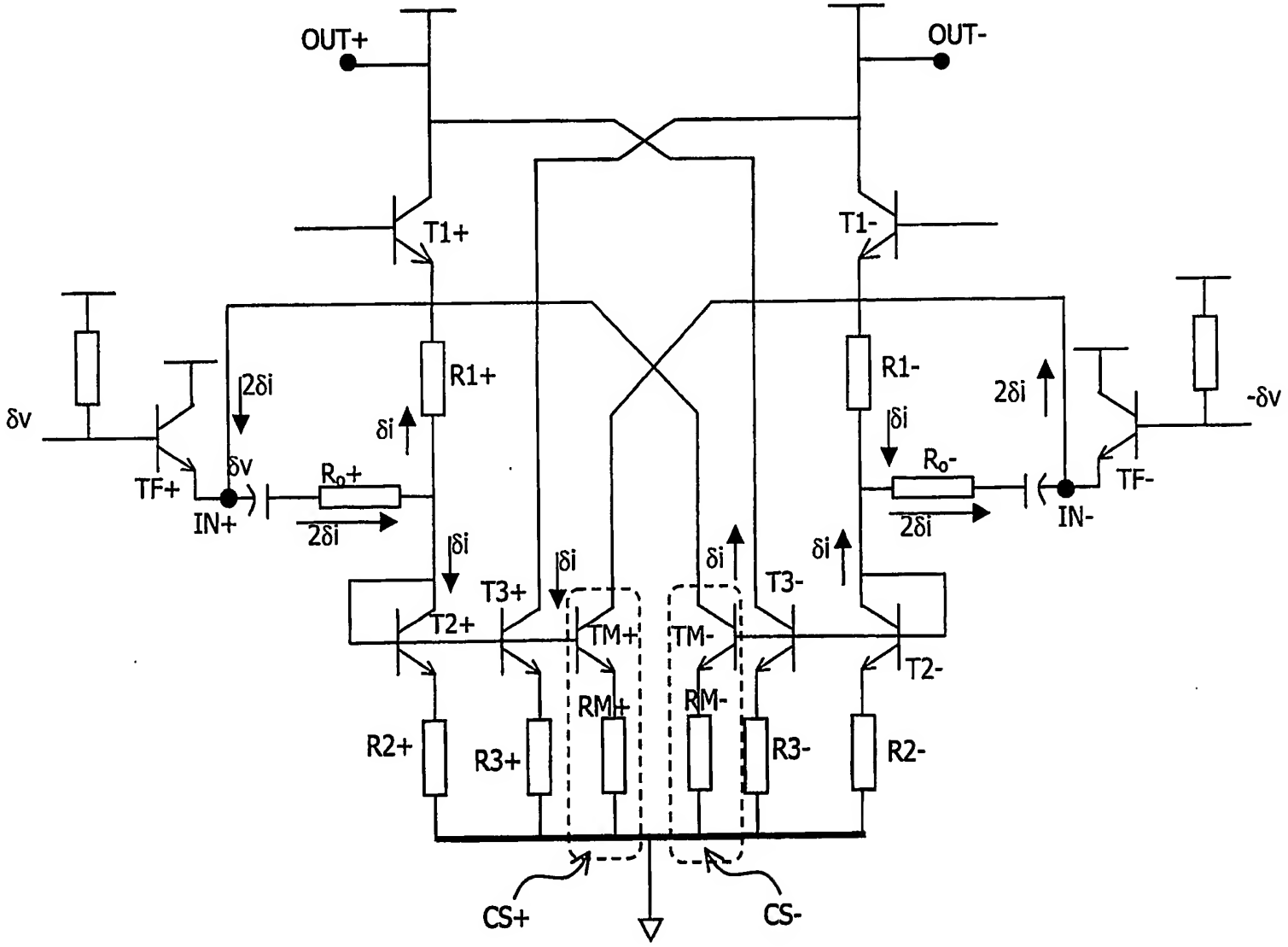

OUT+
OUT-
2δi
2δi
T1+
T1-
Vbias
Vbias
R1+
R1-
IN+
IN-
δi
δi
+δv
-δv
R_o+
R_o-
I_o+2δi
2δi
2δi
I_o-2δi
I_o=Ibias
I_o
δi
δi
δi
δi
T2+
T3+
T3-
T2-
R2+
R3+
R3-
R2-
PST

FIG. 1


OUT+
OUT-
T1+
T1-
R1+
R1-
δv
2δi
δi
TF+
TF-
IN+
IN-
R_o+
R_o-
T3+
T3-
T2+
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TM-
RM+
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R2+
R3+
R3-
R2-
CS+
CS-

FIG. 2

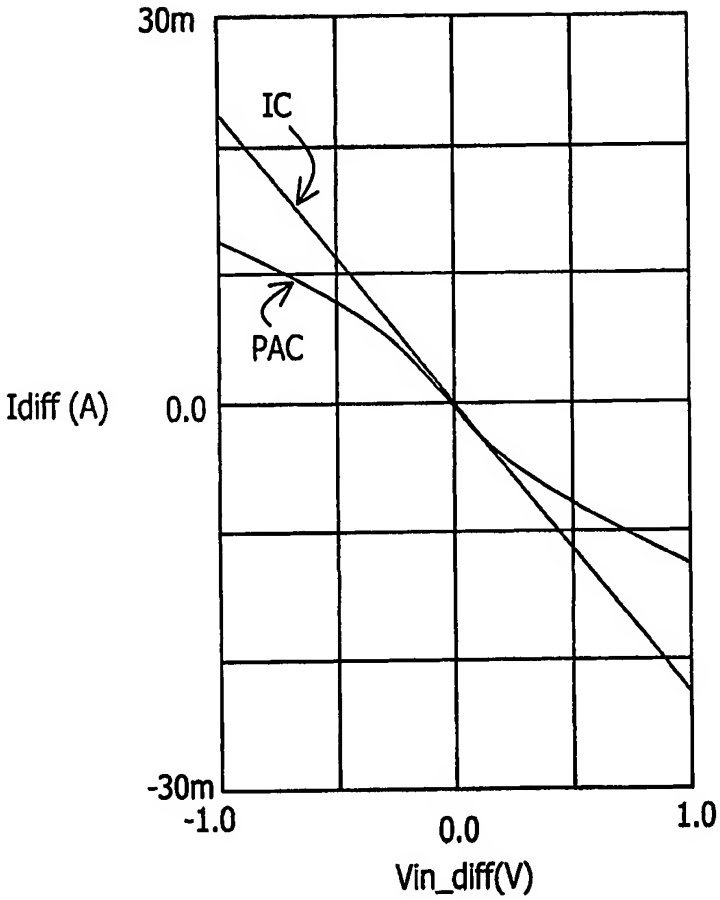
30m
IC
PAC
Idiff (A)
0.0
-30m
-1.0
0.0
1.0
Vin_diff(V)

FIG. 3a

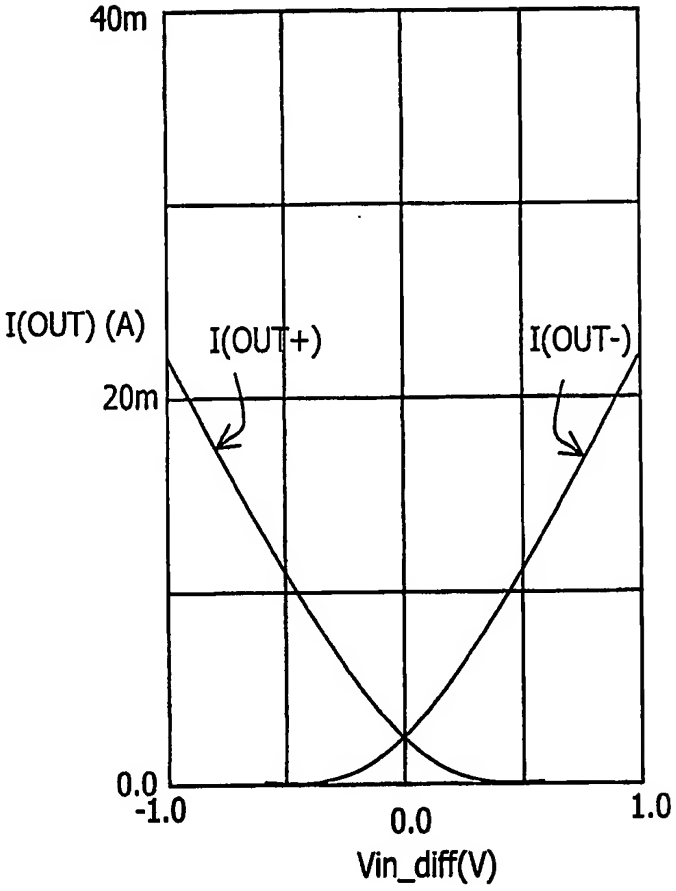
40m
I(OUT) (A)
I(OUT+)
I(OUT-)
20m
0.0
-1.0
0.0
1.0
Vin_diff(V)

FIG. 3b

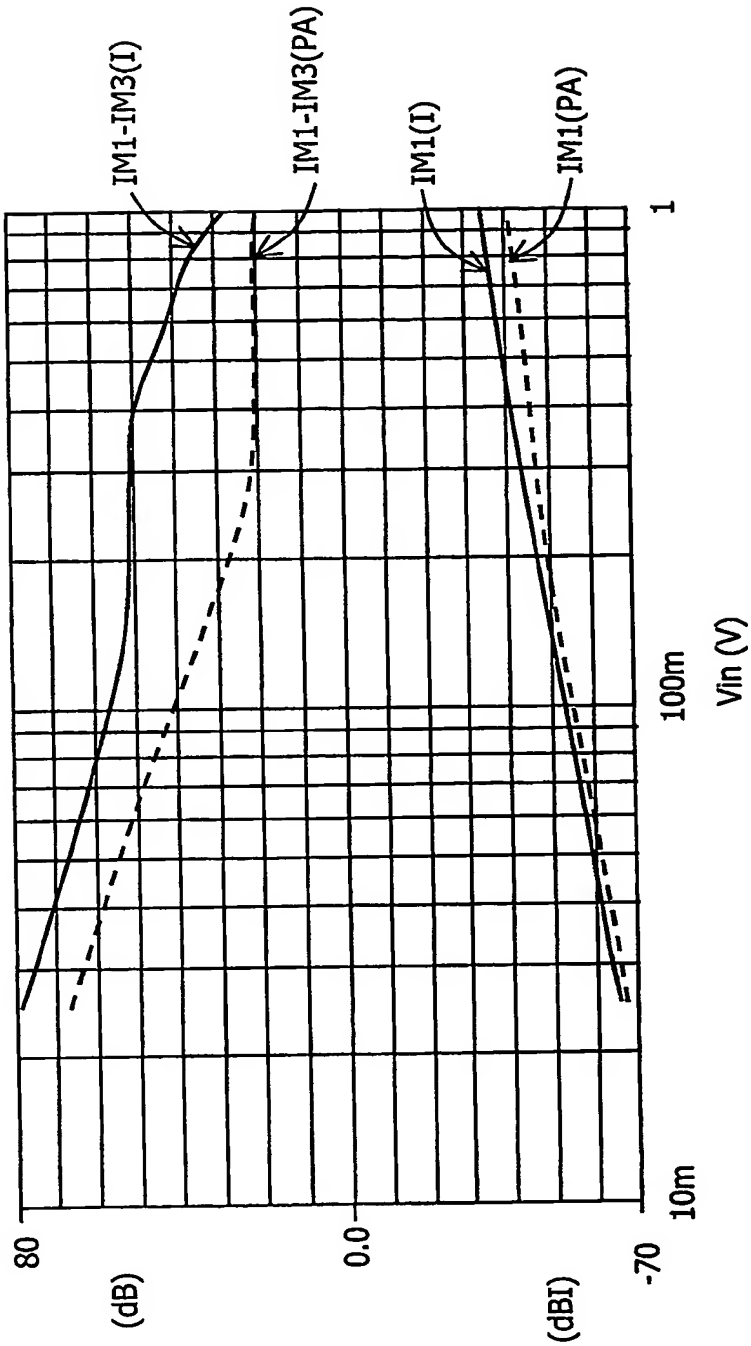

FIG. 4

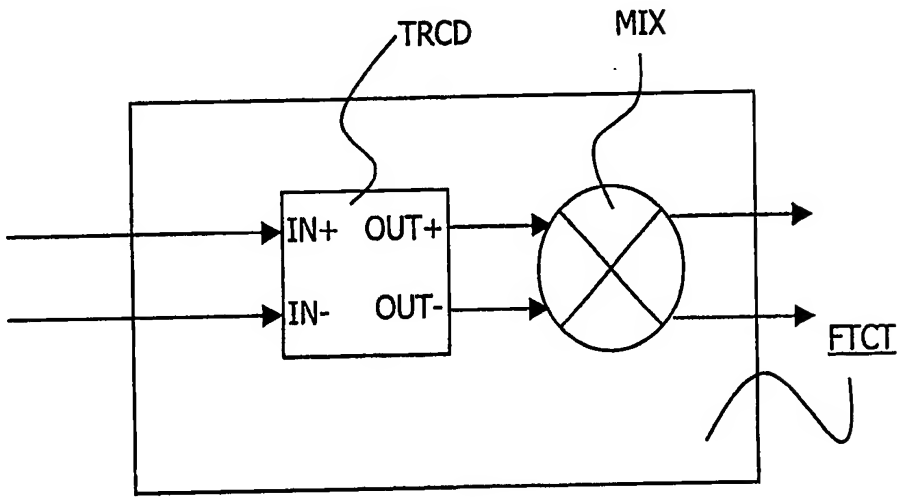

FIG. 5

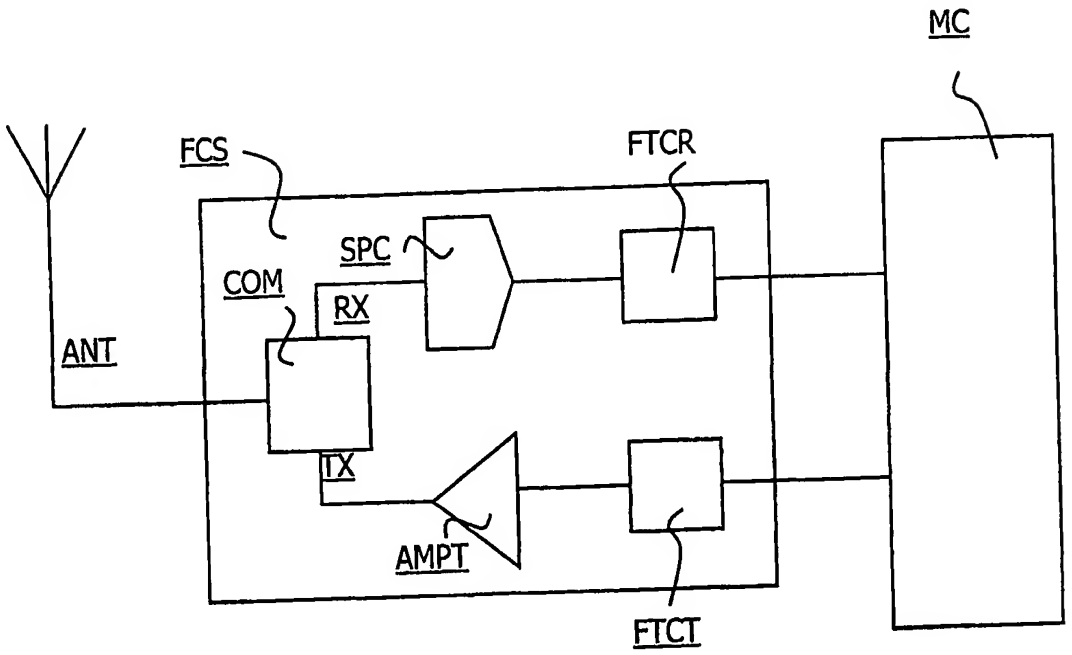

FIG. 6